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(54) **A PROCESSOR PROVIDED WITH A SLOW-DOWN FACILITY THROUGH PROGRAMMED STALL CYCLES**

PROZESSOR MIT GESCHWINDIGKEITSVERRINGERUNG DURCH PROGRAMMIERTEN HALTZYKLUS

PROCESSEUR AYANT UNE FONCTION DE RALENTISSEMENT GRACE A DES CYCLES DE TEMPORISATION PROGRAMMES

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Description

BACKGROUND OF THE INVENTION

[0001] The invention relates to a processor according to the preamble of Claim 1 hereafter appended. At present, there is a trend in circuitry design towards building a so-called **D**igital **V**ideo **P**latform **(DVP)** that will perform various multimedia-processing functions. Such functions may be effected in hardware, in software, or in a mixture thereof, such choice depending on the processing function itself, and/or on the manufacturing volume of the function and/or circuit in question. The multimedia may include video, graphics, audio, or other.

[0002] US 5,175,844 refers to an execution rate controlling device that periodically supplies a hold demand signal to suspend the processing operation during reception of the hold demand signal and comprises a data holding unit for holding held data representative of the execution rate. A generating unit generates the hold demand signal in response to the held data and the clock signal so that the hold demand signal may last for a duration which is inversely proportional to the execution rate. The generating unit comprises a counter unit for counting a count in synchronism with the clock signal up to a maximum value defining a period of periodic supply of the hold demand signal, and produces counted data indicative of the count and a carry signal initializing the count to zero when the count reaches the maximum value. A comparing unit compares the held data with the counted data and produces a coincidence signal when the held data and the counted data coincide with each other. A supplying unit supplies the hold demand signal to the central processing unit from a time instant of reception of the coincidence signal to a time instant of reception of a carry signal.

[0003] In US 4,981,296, a data processing machine is provided with a microprocessor that functions in response to signals output by a clock oscillator to selectively change the data-processing speed of the microprocessor. The data processing machine contains a circuit for generating interruption signals at specific intervals by dividing the signals output by the clock oscillator, a signal-input device for inputting command signals that cause the microprocessor to change the data-processing speed, and a controller which, in response to signals from the input device, executes a stand-by process each time a specific number of interruption signals generated by the interruption signal generating circuit is received.

[0004] For reasons of economy, quite often such processor will be dedicated to the execution of only a limited subset of those functions, often even to executing only a single one function. This policy will render a shared bus that connects the various processors to a background memory a key facility of an overall processing system. Now, for controlling the overall system, often furthermore a **C**entral **P**rocessing **U**nit **(CPU)** will be provided. Next to controlling the background memory, the CPU may immediately access various control registers in the various processors. The number of such processors in realistic systems may have risen to 10-20.

[0005] The present invention is directed to solving a problem that has been recognized when designing a multi-function coprocessor that is able to perform both **M**otion **E**stimation **(ME)** and **M**otion **C**ompensation **(MC)**. These functions are used in video format conversion systems; some examples of such systems have been described by G. de Haan, et al., in an article "True motion estimation with 3-D recursive block batching", IEEE Trans CSVT, Oct. 1993, p. 368.388. In a complex system like this, the prevailing bandwidth on the shared bus is a prime design issue, and the various processors should maintain synchronization on the time slot level of the processing of an entire field or frame.

SUMMARY TO THE INVENTION

[0006] In consequence, amongst other things, it is an object of the present invention to allow programmable slowdown of one or more of the processors being effected in a straightforward manner. Now therefore, according to one of its aspects the invention is characterized according to the characterizing part of Claim 1. The inclusion of stalling cycles will appreciably lower busload, leaving free the remainder of the bus capacity that may be applied to other purposes.

[0007] Advantageously, the programming means are arranged according to Claim 7. This is a straightforward and hardware-efficient solution.

BRIEF DESCRIPTION OF THE DRAWING

[0008] These and further aspects and advantages of the invention will be discussed more in detail hereinafter with reference to the disclosure of preferred embodiments, and in particular with reference to the appended Figures that show:

Figure 1, a general block diagram of a video processing system;
Figure 2, a multiprocessor chip embodying the present invention;
Figure 3, a programmable video processor according to the present invention;
Figure 4, an embodiment of a programming accumulator.
Figure 5, a Table showing Highway Transfer Data for a standard-size scalable pixel block;
Figure 6, a further Table showing Data Rates during ME/MC for implementing such scalability.

DETAILED DESCRIPTION OF PREFERRED EMBODIMENTS

[0009] Figure 1 illustrates a general block diagram of a video processing system. In this conceptual arrange-

ment, signal sources, and in particular, video sources 42, 44, will present video images for processing onto input communication facility 41 that may be a bus or another sharing organization among various stations. Item 20 is a processing chip, which will be discussed more in detail hereinafter, and which will process the images as received. To this effect, chip 20 is associated to RAM 22 that may store an appropriate amount of information to smoothingly cope with peak flows from sources 42, 44, and as the case may be, with peak requests from video users 46, 48. The latter will use video images as having been processed by chip 20. To this effect, items 20, 46, 48, are mutually interconnected through output communication facility 45 that may be a bus or may be sharing among stations in another manner.

[0010] Figure 2 illustrates a multiprocessor chip that is arranged for executing the processing and therewith embodying the present invention. Apart from the Random Access Memory 22, the remainder of the Figure has been compacted into a Single Solid State chip 20. Within this chip, interfacing between bus facility or Onchip Data HighWay 28 and memory 22 is by way of Main Memory Interface 24 and Bus Arbiter 26. Further bus-connected subsystems are Video Input Interface 30, Memory Based Scaler 32, Video Output Interface 34, Central Processing Unit 38 and Processor 36 that executes both Motion Estimation and Motion Compensation. By themselves, M.E. and M.C. are common features of processing a multi-image sequence such as a film or animation, and the associated procedures will not be discussed herein for reasons of brevity. The same applies to the overall image processing functionality to be provided by processor 36 and the hardware and software facilities necessary therefor.

[0011] For discussing the relevance of the data transfer on the bus facility, various modes of use will be considered. Now, the processor 36 may operate in a time-multiplexed manner on ***three*** prime tasks. First, it calculates the motion vectors of an applicable image (ME), then it performs motion compensation on the luminance signal (MC-Y), and finally, it performs motion compensation on the chrominance signal (MC-UV). In principle, the processing block in question may handle an image of arbitrary size, but in the embodiment the maximum throughput is two video streams of 512*240 pixels at 60 Hz, or alternatively 512*288 pixels at 50 Hz. A particular standardized stream amounts to 720*240 pixels at 60 Hz, or alternatively, 720*288 pixels at 50 Hz.

[0012] Examples of use are defined by various operational parameters. The actual ***display mode*** determines which conversion must be executed, which is usually a fixed property of a particular video product once it has been designed, inasmuch as changing of the display scan format is often unviable. The display mode has the following parameter values for determining the actual conversion. Note that the selecting and management among all of these cases is controlled by the CPU, and some of these selection and management functionalities may even be changed dynamically, during run-time. Applicable data rates are as follows

- 50 i / 60 i = 1 times the data rate
- 100 i / 120 i = 2 times the input data rate;
- 100 p / 120 p = 4 times the input data rate.

[0013] The ***scalability mode*** allows the application to effect a trade-off between image quality and the amount of resources used, such as highway bandwidth and available amount of background memory. This effectively controls the quality attained versus the resources that are availble. Various possibilities are as follows:

- frm - fld - fld , previous frame, current field, and next field;
- frm - fld , previous frame and current field
- fld - fld , previous field and current field

[0014] The ***data mode*** controls the amount of video that must be processed, such as only one main widow, as distinct from a background combined with a picture-in-picture display. Various possibilities are:

- one "standard" stream of 720 pixels width
- two "small" streams of 512 pixels width
- Anything else that may lie within the maximum supported image size

[0015] The block 36 has been designed in the embodiment with the following properties:

- Motion estimation requires 1024 cycles to process 128 x 8 pixels
- Motion compensation requires 1600 cycles to process 128 x 8 pixels

[0016] The clock frequency is 150 MHz.

[0017] Figure 3 illustrates a programmable video processor according to the present invention. Within processor 50 there is an interface 62 for communicating with other subsystems such as those shown in Figure 2. Internal communication is effected by internal local bus 60. The various stations or facilities connected thereto are program ROM 52, programmable PROM 54 for storing program and/or data, data RAM 58, and finally processing element 56 that has both input and output coupled to the local bus 60.

[0018] A key item in the processing element is register file 57, that is loadable from bus 60 as shown. Various further control, address, and data interconnection lines have been ignored for brevity, inasmuch as they would represent straightforward solutions to persons skilled in the art. Regarding the overall set-up in Figure 2, the data inputs and outputs functionally connect to data highway 28. The control input, including the bading of register file 57 is typically fed by CPU 38. The CPU can set various bits in register file 57. Data will be received from shared

memory, processed by the coprocessing element, and the results thereof will be stored in the shared memory. Typically, the processing constitutes a parameterized data pipe, that has its processing parameters read from the control register file. The pending on the various control bits, one or more data inputs and/or outputs may be activated. Also the function being performed depends on such control bits.

[0019] Fig. 4 illustrates an embodiment of a programming accumulator. Herein, a programming register 72 is loaded via line 70 with a first number. Under clock synchronization, the register content is forwarded to adder 74 for addition to the content of accumulator register 76, the content being retrocoupled through interconnection 78. The sum of the two data is written back to accumulator storage facility 76. Now, the higher the content of register 72, the more frequently carry output 80 from accumulator 76 generate a carry signal. The carry signal may then control an effective clock cycle for therewith having execute the processor of the present invention an image processing. However, in the preferred embodiment of the present invention, the carry signal will control a stall cycle where in no effective data processing is done. Therefore, as more frequent carry signals will be present, the more stall cycles will be inserted, effectively slowing down the date processing by the coprocessor. An additional reason for preferring the latter embodiment is that it would allow the carry signals to be ORED with other causes for stalling, such as FIFO overflow in the processing element's output or FIFO underflow in the processing element's input.

[0020] Fig. 5 is a Table showing Highway Transfer Data for a standard-size scalable pixel block of 128 X 8 pixels, during motion-estimation and motion compensation for the various display modes. Motion estimation and motion compensation require approximately the same input data but produce different output data, and also different amounts of output data. Clearly, the total variation is about + 50% in the rightmost column.

[0021] Figure 6 is a further Table showing Data Rates during ME/MC for such scalability, and in particular, the consequences arising for the highway bandwidth during ME and MC for the various display modes recited supra. In a typical system, the memory is operating at 166 MHz, 32 bits dual data rate, which results in a theoretical maximum highway bandwidth of
(166 * 2 * 4) or approximately 1200 Mbyte/sec.

[0022] During ME, the throughput requirement is 732 Mbyte/sec. This bandwidth should therefore in principle being continually available, even in a relatively slow 50i/60i system. On the other hand, one would wish that such relatively slow system should be able to operate at a lowered data rate in comparison with the modes requiring higher display rates. In fact, one should wish to relinquish a certain amount of bandwidth, at a cost of a few extra clock cycles. In consequence, the present invention offers a ***programmable*** slow down facility, inasmuch as the optimum would depend on the actual display mode. A further requirement is to have the present invention introduce a facility to save bandwidth also for the processing of smaller images.

[0023] The present invention will therefore offer a programmable slowdown factor in the digital circuitry of the coprocessor. For a slowdown factor of S, that is any real number, ≥ 1, the following holds:

- Motion Estimation requires S * 1024 cycles to process 128 * 8 pixels;
- Motion Compensation requires S * 1600 cycles to process 128 * 8 pixels.

[0024] On the basis of the software governing the display motion, the slowdown factor will be easily set in this manner. An advantageous embodiment is through an accumulator that periodically accumulates an appropriate operand. The carry output will rise to high whenever the accumulator overflows. The carry out will be controlled by the overflows/wraps, for thereby controlling the stalling of the overall processor. Giving a few embodiments hereinafter for Motion Estimation would render the presenting of similar measures for Motion Compensation superfluous.

[0025] For a value of S =1.215, we want 1024 * 1.215 = 1244 cycles to compute 128 * 8 pixels. That means that we want stalling 1244 -1024 = 220 times in a 1244 cycle interval. The correct programming would therefor be **x** =220 / 1244 = 0.1768489.

[0026] For a value of S = 16, we want 1024 * 16 = 16384 cycles to compute 128 * 8 pixels. That means that we want stalling 16384 -1024 =15360 times in a 16384 cycle interval. The correct programming would therefor be **x** =15360 / 16384 = 0.9375. Clearly, **X = (S -1)** / **S.** Implementing a long accumulator register will allow accurate programming of the required factor. A 10-bit accumulator has the parameter N to be set by the CPU to control the programmable slowdown: **N** = **round (1024 * x).** For the two factors supra, such will result in the following:

S = 1.215; x = 0.1768489; N = 181.
S = 16; x = 0.9375; N = 960.

[0027] Various other floating points to integer conversions could also be used to generate the stall cycles. A case in point is to do so whilst using a truncation operation.

[0028] A further advantage of the programmable stalling according to the preceding is that it will allow other bus master stations, such as other coprocessors that have a lower priority than memory, to have relatively smaller buffers than would have been the case otherwise. Especially in the interval during which the stalling processor does not access the bus, lower priority master stations will be periodically allowed to temporarily grab the bus. In fact, this feature leads to smaller IC area, and inherently, to lower manufacturing costs.

[0029] The programmable processing slowdown of the present invention allows for still another advantageous feature. As has been mentioned supra, other causes for stalling could be present, such as buffer overflow and/or underflow. Still another cause would be represented by excessive highway latency, such as through bus loading by other coprocessors. For these latter causes, generally only a limited time budget is available. If however, this time budget is exceeded, the coprocessor according to the present invention will not be finished in time, which in a prior art system represents a failure.

[0030] Therefore, according to a preferred embodiment of the present invention, an extra interrupt signal would be generated when the number of these extra stalls, i.e., other than currently programmed, exceeds a predetermined threshold. This further interrupt will then start a feedback that may decrease the slowdown factor associated with the programmed slowdown. This may be done by amending the recurrency of the stall cycles, such as through addressing another item in register file 57 in Figure 3. Another solution is by having the bus arbiter allocate more bandwidth to the coprocessor according to the present invention.

[0031] In fact, the hardware itself could adjust its stalling recurrency by undertaking to maintain a programmable constant stall rate. If such cannot be achieved through excessive highway latency, the hardware could interrupt the processor. The processor could then allocate more bandwidth to the coprocessor by reprogramming the arbiter to another allocation parameter value. Still another approach is to amend the overall control parameters of the coprocessor to exploit its scalability, such as by falling back to a three-field mode for motion compensation to guarantee that everything gets computed within the available time schedule.

[0032] The above embodiments of the invention have been presented by way of examples, rather than by way of limitation. In consequence, persons skilled in the art will recognize various changes and amendments that would not exceed the scope of the invention, inasfar as such scope has been covered by the appended Claims. In particular, the invention may be applied in other field that use signal processing, such as applied to audio, graphics, and other.

Claims

1. A processor (20) for executing digital signal processing under control of a clock facility, such that a sequence of C effective clock cycles will effect a processing operation of a predetermined amount of digital signal information,
said processor further having programming means (72) for implementing programmable stall clock cycles interspersed between said effective clock cycles for implementing a programmable slowdown factor **S**, such that a modified number of **C*S** overall clock cycles will effect processing of said predetermined amount of digital signal information, the processor being **characterized in that** said programming means (72) are adapted to drive an incrementable storage facility (76) through a periodical increment by a number N that is a function of said factor **S** according to **N = round (R * x),** wherein **x = (S -1/S)** and **R** is the range of the storage facility, and adapted to generate a stall cycle from a carry output signal of the storage facility.

2. A processor as claimed in claim 1, and having said programming means controlling the interspersing in an at least periodical manner.

3. A processor as claimed in claim 1, effectively representing a coprocessor and having a control processor as said programming means.

4. A processor as claimed in claim 3, wherein said coprocessor and said control processor are interconnected by a bus to a shared memory facility.

5. A processor as claimed in claim 4, wherein said coprocessor, said control processor and said bus are disposed on a single semiconductor chip, whereas said shared memory facility is off-chip.

6. A processor as claimed in claim 1, and being arranged to execute at least two different modes, the modes being **characterized by** requiring respective different amounts of data to be processed under respective different percentages of stall clock cycles.

7. A processor as claimed in claim 1, said stall cycles being generated by a floating point to integer conversion, wherein said conversion is an approximation of a required increment or decrement of an accumulator.

8. A processor as claimed in claim 1, wherein said programming means drive an arithmetic element that is arranged for executing an addition or subtraction operation with regard to a programmed value, and said addition or subtraction will in a first case produce a carry or borrow signal, respectively, and in a second case not produce such carry signal or borrow signal, respectively, and wherein a transition from a stall cycle to an effective processing cycle will be controlled by a transition between said first and second states.

9. A processor as claimed in claim 5, wherein at least one other bus station than the coprocessor is allowed to grab the bus in a time interval during a said stall cycle.

10. A processor as claimed in claim 1, furthermore hav-

ing an origin for controlling second stall cycles, and comprising a detection facility for detecting an excessive number of said programmable stall cycles and said second stall cycles combined, and said processor having a control facility fed by said detection facility for then amending a recurrency of said programmable stall cycles.

11. A processor as claimed in claim 10, wherein said detection facility is arranged for generating an interrupt signal.

12. A processor as claimed in claim 10, wherein said detection facility is arranged for letting a bus arbiter allocate more bandwidth to the coprocessor in question.

13. A processor as claimed in claim 1, furthermore having an origin for controlling second stall cycles, and comprising a detection facility for detecting an excessive number of said programmable stall cycles and said second stall cycles combined, and said processor having a control facility fed by said detection facility for then amending one or more control parameters of the coprocessor through exploiting its scalability.

Patentansprüche

1. Prozessor (20) zur Ausführung digitaler Signalverarbeitung unter Steuerung einer Takteinrichtung, so dass eine Sequenz von **C** effektiven Taktzyklen einen Verarbeitungsvorgang einer vorbestimmten Menge von Digitalsignalinformationen beeinflusst, wobei der genannte Prozessor ferner Programmiermittel (72) zum Implementieren von zwischen den genannten effektiven Taktzyklen eingestreuten programmierbaren Wartetaktzyklen zum Implementieren eines programmierbaren Verlangsamungsfaktors **S** hat, so dass eine modifizierte Zahl von **C*S** Taktzyklen insgesamt die Verarbeitung der genannten vorbestimmten Menge von Digitalsignalinformationen beeinflusst, wobei der Prozessor **dadurch gekennzeichnet ist, dass** die genannten Programmiermittel (72) zum Ansteuern einer inkrementierbaren Speichereinrichtung (76) durch ein periodisches Inkrement um eine Zahl **N** ausgeführt sind, die eine Funktion des genannten Faktors **S** gemäß **N** = **round (R*x)** ist, wobei **x** = **(S - 1/S)** und **R** der Bereich der Speichereinrichtung ist, und zum Erzeugen eines Wartezyklus von einem Übertragausgangssignal der Speichereinrichtung ausgeführt ist.

2. Prozessor nach Anspruch 1 und bei dem die genannten Programmiermittel das Einstreuen in einer wenigstens periodischen Weise steuern.

3. Prozessor nach Anspruch 1, der effektiv einen Coprozessor repräsentiert und einen Steuerungsprozessor als das genannte Programmiermittel hat.

4. Prozessor nach Anspruch 3, bei dem der genannte Coprozessor und der genannte Steuerungsprozessor durch einen Bus mit einer gemeinsam genutzten Speichereinrichtung verbunden sind.

5. Prozessor nach Anspruch 4, bei dem der genannte Coprozessor, der genannte Steuerungsprozessor und der genannte Bus auf einem einzelnen Halbleiterchip angeordnet sind, während die genannte gemeinsam genutzte Speichereinrichtung chip-extern ist.

6. Prozessor nach Anspruch 1 und zur Ausführung von wenigstens zwei verschiedenen Modi angeordnet ist, wobei die Modi **dadurch gekennzeichnet sind, dass** sie erfordern, dass jeweilige verschiedene Datenmengen unter jeweiligen verschiedenen Prozentanteilen von Wartetaktzyklen verarbeitet werden.

7. Prozessor nach Anspruch 1, bei dem die genannten Wartezyklen durch eine Umwandlung von Gleitkomma in Ganzzahl erzeugt werden, wobei die genannte Umwandlung eine Näherung eines erforderlichen Inkrements oder Dekrements eines Akkumulators ist.

8. Prozessor nach Anspruch 1, bei dem die genannten Programmiermittel ein arithmetisches Element ansteuern, das zur Ausführung eines Additions- oder Subtraktionsvorgangs in Bezug auf einen programmierten Wert angeordnet ist, und die genannte Addition oder Subtraktion in einem ersten Fall ein Übertrag- bzw. Vortragsignal erzeugt und in einem zweiten Fall kein derartiges Übertrag- bzw. Vortragsignal erzeugt und bei dem ein Übergang von einem Wartezyklus zu einem effektiven Verarbeitungszyklus von einem Übergang zwischen dem genannten ersten und zweiten Zustand gesteuert wird.

9. Prozessor nach Anspruch 5, bei dem wenigstens eine weitere Busstation als der Coprozessor in einem Zeitintervall während eines genannten Wartezyklus auf den Bus zugreifen darf.

10. Prozessor nach Anspruch 1, der des Weiteren einen Ursprung zur Steuerung von zweiten Wartezyklen hat und eine Detektionseinrichtung zum Detektieren einer übermäßigen Zahl der genannten programmierbaren Wartezyklen und der genannten zweiten Wartezyklen zusammen aufweist und wobei der genannte Prozessor eine Steuerungseinrichtung hat, die von der genannten Detektionseinrichtung gespeist wird, um dann ein Wiederauftreten der genannten programmierbaren Wartezyklen zu ändern.

11. Prozessor nach Anspruch 10, bei dem die genannte Detektionseinrichtung zur Erzeugung eines Interrupt-Signals angeordnet ist.

12. Prozessor nach Anspruch 10, bei dem die genannte Detektionseinrichtung so angeordnet ist, dass sie einen Busarbiter einem betreffenden Coprozessor mehr Bandbreite zuteilen lässt.

13. Prozessor nach Anspruch 1, der des Weiteren einen Ursprung für die Steuerung von zweiten Wartezyklen hat und eine Detektionseinrichtung zum Detektieren einer übermäßigen Zahl der genannten programmierbaren Wartezyklen und der genannten zweiten Wartezyklen zusammen aufweist und wobei der genannte Prozessor eine Steuerungseinrichtung hat, die von der genannten Detektionseinrichtung gespeist wird, um dann einen oder mehrere Steuerparameter des Coprozessors durch Nutzen seiner Skalierbarkeit zu ändern.

Revendications

1. Processeur (20) pour exécuter un traitement de signaux numériques sous la commande d'une fonction d'horloge, de telle sorte qu'une séquence de C cycles d'horloge effectifs C affecte une opération de traitement d'une quantité prédéterminée d'informations de signaux numériques,
ledit processeur ayant en outre des moyens de programmation (72) pour mettre en oeuvre des cycles d'horloge de temporisation programmables intercalés entre lesdits cycles d'horloge effectifs pour mettre en oeuvre un facteur de ralentissement programmable **S,** de telle sorte qu'un nombre modifié de **C*S** cycles d'horloge globaux affectent le traitement de ladite quantité prédéterminée d'informations de signaux numériques, le processeur étant **caractérisé en ce que** lesdits moyens de programmation (72) sont adaptés pour commander une fonction de mémorisation incrémentable (76) par le biais d'un incrément périodique par un nombre **N** qui est fonction dudit facteur **S** selon **N** = **arrondi (R*x),** où **x** = **(S - 1** / **S)** et **R** est la plage de la fonction de mémorisation, et adaptés pour générer un cycle de temporisation à partir d'un signal de sortie de report de la fonction de mémorisation.

2. Processeur selon la revendication 1, dont lesdits moyens de programmation commandent l'intercalage au moins d'une façon périodique.

3. Processeur selon la revendication 1, représentant en fait un coprocesseur et ayant un processeur de commande comme dits moyens de programmation.

4. Processeur selon la revendication 3, dans lequel ledit coprocesseur et ledit processeur de commande sont interconnectés par un bus à une fonction de mémoire partagée.

5. Processeur selon la revendication 4, dans lequel ledit coprocesseur, ledit processeur de commande et ledit bus sont disposés sur une même puce à semiconducteur, tandis que ladite fonction de mémoire partagée est hors puce.

6. Processeur selon la revendication 1, agencé pour exécuter au moins deux modes différents, les modes étant **caractérisés en ce qu'**ils exigent des quantités respectives différentes de données à traiter dans des pourcentages respectifs différents de cycles d'horloge de temporisation.

7. Processeur selon la revendication 1, lesdits cycles étant générés par une conversion de virgule flottante en nombre entier, dans lequel ladite conversion est une approximation d'un incrément ou décrément requis d'un accumulateur.

8. Processeur selon la revendication 1, dans lequel lesdits moyens de programmation commandent un élément arithmétique qui est agencé pour exécuter une opération d'addition ou de soustraction concernant une valeur programmée, et ladite addition ou soustraction dans un premier cas produira un signal de report ou de retenue, respectivement, et dans un second cas ne produira pas de tel signal de report ou signal de retenue, respectivement, et dans lequel une transition d'un cycle de temporisation à un cycle de traitement effectif sera commandée par une transition entre lesdits premier et second états.

9. Processeur selon la revendication 5, dans lequel au moins une station de bus autre que le coprocesseur est autorisée à saisir le bus dans un intervalle de temps durant un dit cycle de temporisation.

10. Processeur selon la revendication 1, ayant en outre une origine pour commander des seconds cycles de temporisation, et comprenant une fonction de détection pour détecter un nombre excessif desdits cycles de temporisation programmables et desdits seconds cycles de temporisation combinés, et ledit processeur ayant une fonction de commande alimentée par ladite fonction de détection pour ensuite modifier une récurrence desdits cycles de temporisation programmables.

11. Processeur selon la revendication 10, dans lequel ladite fonction de détection est agencée pour générer un signal d'interruption.

12. Processeur selon la revendication 10, dans lequel ladite fonction de détection est agencée pour laisser

un arbitre de bus allouer une plus grande largeur de bande au coprocesseur en question.

13. Processeur selon la revendication 1, ayant en outre une origine pour commander des seconds cycles de temporisation, et comprenant une fonction de détection pour détecter un nombre excessif desdits cycles de temporisation programmables et desdits seconds cycles de temporisation combinés, et ledit processeur ayant une fonction de commande alimentée par ladite fonction de détection pour ensuite modifier un ou plusieurs paramètres de commande du coprocesseur en exploitant son extensibilité.

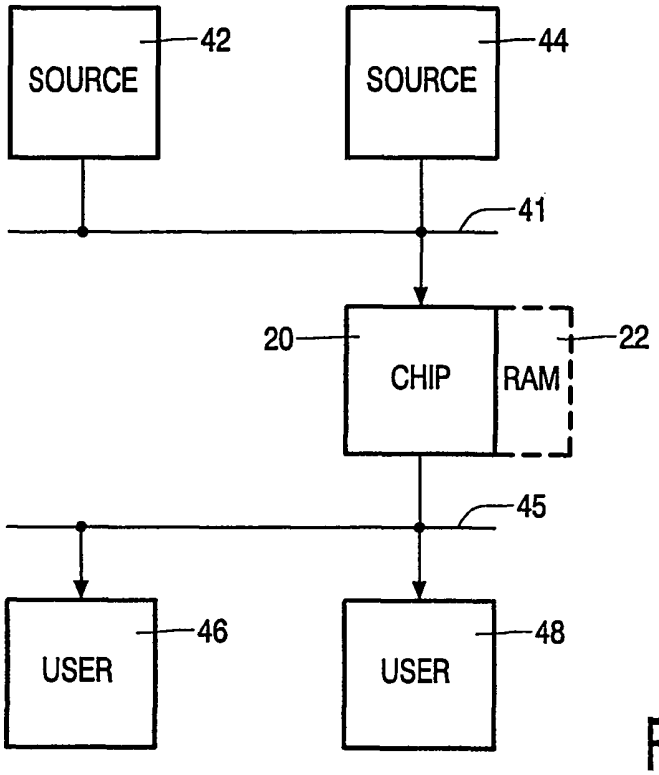
SOURCE
42
SOURCE
44
41
20
CHIP
RAM
22
45
USER
46
USER
48

FIG. 1

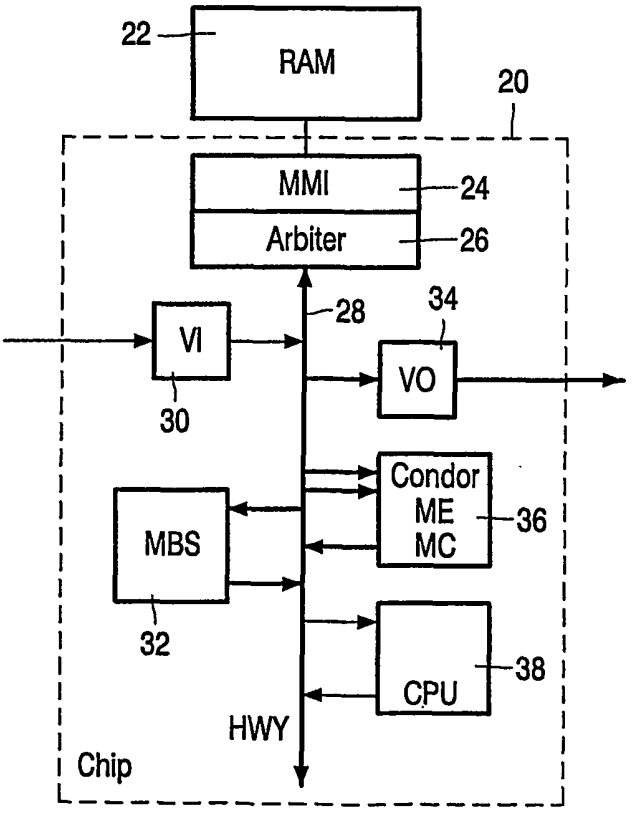
22
RAM
20
MMI
24
Arbiter
26
28
34
VI
VO
30
Condor
ME
MC
36
MBS
32
CPU
38
HWY
Chip

FIG. 2

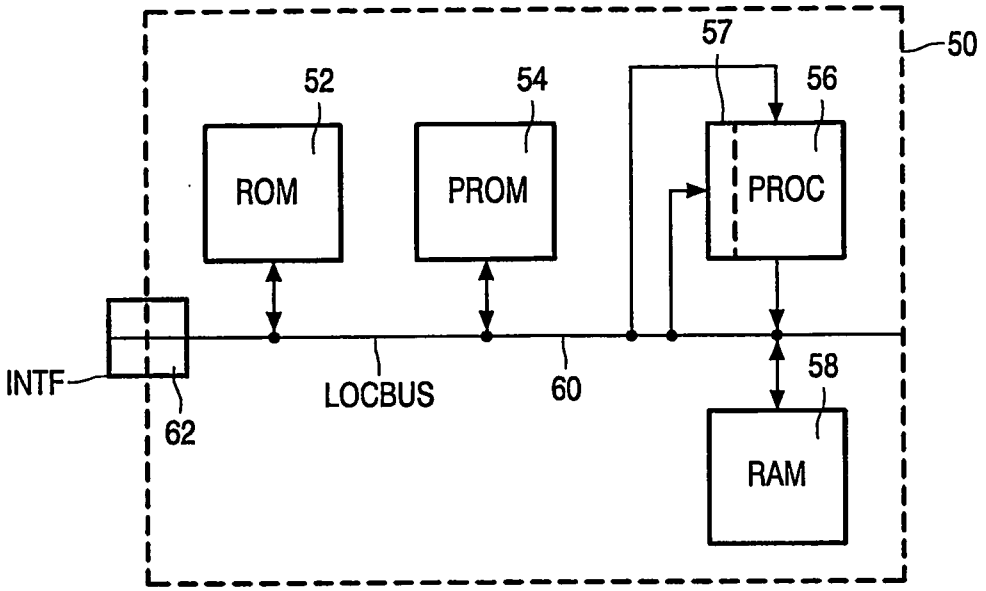
57
50
52
54
56
ROM
PROM
PROC
INTF
62
LOCBUS
60
58
RAM

FIG. 3

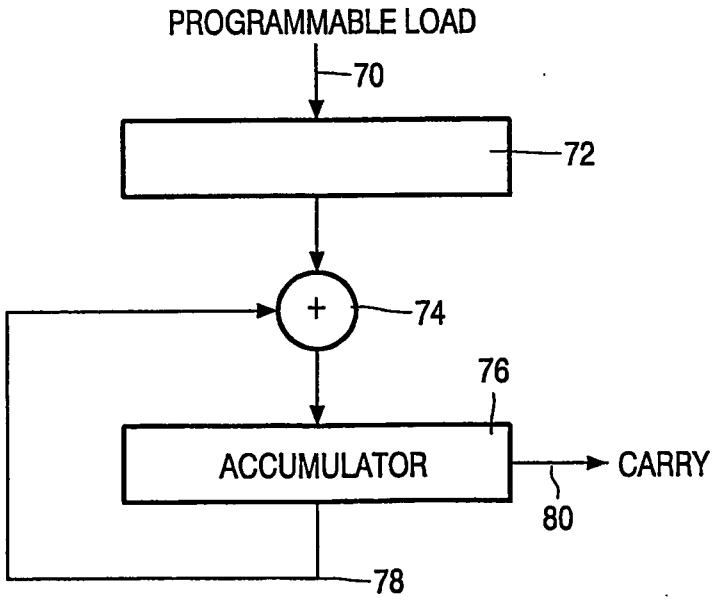
PROGRAMMABLE LOAD
70
72
+
74
76
ACCUMULATOR
CARRY
80
78

FIG. 4

Table 1 Highway data transfers for 128x8 pixels for frm-fld scalability

	ME	MC with 50i/60i output	MC with 100i/120i or 50p/60p output	MC output 100p/120p
Prev. frame input	2 x 8	2 x 8	2 x 8	2 x 8
Curr. field input	2 x 4	2 x 4	2 x 4	2 x 4
Next frame input	2 x 4	2 x 4	2 x 4	2 x 4
Vector input	4	1	1	1
Vector output	1			
SAD best output	1			
SAD sel. output	1			
Rec. frame output		8	8	8
Both display outputs		4	8	2 x 8
Total Transfer	**39**	**45**	**49**	**57**
Total Bytes [a]	**4992**	**5760**	**6272**	**7296**

a. All transfers are 128 bytes.

FIG. 5

Table 2 Data rates during ME/MC for frm-fld-fld scalability

	ME	MC 50i/60i	MC 100i/120i or 50p/60p	MC 100p/120p
Bytes	4992	5760	6272	7296
Cycles	1024	1600	1600	1600
Bytes/Cycle	4.88	3.60	3.92	4.56
MBytes/sec.	732	540	588	684

FIG. 6

REFERENCES CITED IN THE DESCRIPTION

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Patent documents cited in the description

- US 5175844 A **[0002]**
- US 4981296 A **[0003]**

Non-patent literature cited in the description

- **G. de Haan et al.** True motion estimation with 3-D recursive block batching. *IEEE Trans CSVT,* October 1993, 368.388 **[0005]**